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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,646	09/17/2003	Yutaka Ohmoto	500.39750VX1	3794

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EXAMINER	
DHINGRA, RAKESH KUMAR	
ART UNIT	**PAPER NUMBER**
1763	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/663,646	OHMOTO ET AL.	
	Examiner	Art Unit	
	Rakesh K. Dhingra	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12,13 and 15-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12,13,15 and 18-20* is/are allowed.

6)☒ Claim(s) *16, 17, 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention as explained hereunder.

Claim 16, line 12 recites "a direct current power source connected between said electrode and said high frequency power source" which is not in line with Figure 10 of the disclosure, where DC power source 47 is connected directly to the electrode 22.

Accordingly for the purpose of examination on merits this limitation is interpreted as "a direct current power source connected between to said electrode".

Applicant is invited to clarify/amend this claim limitation.

Response to Arguments

Applicant's arguments with respect to claims 12, 13, 15-19 have been considered and following response is given:

Amended claim 12 is indicated as allowable subject matter. Claims 13, 15, 18-20 are also indicated as allowable subject matter, being dependent upon claim 12.

As regards amended claim 16, new reference (US patent No. 6,268,994 – Logan et al) has been found that when combined with Ogahara and Sill et al reads on the claim limitations. Accordingly claims 16, 17 and 20 have been rejected under 35 USC 103 (a) as explained below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Logan et al (US Patent No. 6,268,994) in view of Ogahara (US Patent No. 5,958,265) and Sill et al (US Patent No. 6,367,413).

Regarding Claim 16: Logan et al teach an apparatus for plasma processing (Figures 1-6) comprising:

a conductive base member 11 (electrode) for an electrostatic chuck

an insulating layer 18 formed on a surface of said electrode 11;

an electrode 20 (conductive material) buried within and surrounded by said insulating layer 18 in a ring-like form;

contact posts 16 for electrically connecting the electrodes 20;

wherein one portion of said insulating layer 18 formed on an outer part of said electrode 11 where said conductive material (electrode 20) buried within and surrounded by said insulating layer 18 has a thickness which is greater than a thickness of another portion of said insulating layer 18 where said conductive material (electrode 20) is not buried and which extends from a central part of said electrode to said one portion of said insulating layer 18 where said conductive material (electrode 20) is buried (column 3, lines 5-62).

Logan et al do not teach a high-frequency power source for applying bias power to the electrode, a substrate to be processed disposed on the electrode, a feeder line connecting the high-frequency power source and the conductive material, a variable capacitor provided in the said feeder line, and a direct current power source connected between the said electrode and the said high frequency power source.

Ogahara teaches a plasma processing apparatus (Figure 1) for processing a product using a plasma comprising:

a power source 6 source for applying bias power to an (holder main body) electrode 1 on which a substrate 10 to be processed is disposed;

a holding plate (insulating layer) 2 formed on a surface of said electrode on which said substrate to be processed is disposed;

a chucking electrode (first conductive material) 61 formed within said insulating layer;

a conductor (first feeder line) 62 connecting said power source and said first conductive material;

a direct current power source 64 connected to the electrode 1 (Ogahara – Figure 1 and column 7, line 10 to Column 8, line 45).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use the substrate holder configuration as taught by Ogahara in the apparatus of Logan et al to enable use the same for plasma processing applications.

Logan et al in view of Ogahara do not teach a variable capacitor provided in the feeder line.

Sill et al teach a plasma apparatus (Figures 1, 2) that includes substrate support 20 with plurality of electrodes 44, 46 that are coupled to RF power source 48 through variable capacitors 56, 58 respectively (Column 6, line 50 to Column 8, line 30).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use variable capacitors for coupling the RF power source to the plurality of electrodes in substrate support as taught by Sill et al in the apparatus of Logan et al in view of Ogahara to enable vary the bias voltage created on the substrate surface (Column 8, lines 5-30).

Regarding Claim 21: Logan et al teach that thickness of another portion of insulating layer 18 is substantially constant (Figure 6).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Logan et al (US Patent No. 6,268,994) in view of Ogahara (US Patent No. 5,958,265) and Sill et al (US Patent No. 6,367,413) as applied to Claim 16 and further in view of Nakano et al (US Patent No. 6,270,618).

Regarding Claim 17: Logan et al in view of Ogahara and Sill et al teach all limitations of the claim including RF filter 64, 66 (could be configured as resonant circuits including resonant coils) connected between DC power source 50 and electrodes 46, 44 (Sill et al – Figure 1, lines.

Logan et al in view of Ogahara and Sill et al do not teach resonant coil connected between feeder line and electrode.

Nakano et al teach an apparatus (Figures 1A, 3) that includes band eliminators (resonance LC circuit) 61b, 61b' where resonance coils L2, L2' are connected between electrode 8 and feeder line [Column 2, lines 40-50 and Column 3, lines 30-65].

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use a resonant circuit (coil and capacitor) as taught by Nakano et al in the apparatus of Logan et al in view of Ogahara and Sill et al to provide resonant coil (band eliminators) to enable trap plasma between plasma excitation electrode and susceptor electrode (Column 3, lines 30-54).

Allowable Subject Matter

Claims 12, 13, 15, 18-20 are allowed.

The following is an examiner's statement of reasons for allowance:

Claim 12: Prior arts (US Patents – 6,268,994 – Logan et al, and US Patent No. 6,188,564 – Hao et al) do not teach claim limitation "wherein one portion of said insulating layer formed on an outer part of said electrode where said first conductive material and said second conductive material are buried within and surrounded by said insulating layer has a thickness which is greater than a thickness of another portion of said insulating layer where said first conducive material and said second conductive material are not buried and which extends from a central part of said electrode to the one portion of said insulating layer where said first conductive material and said second conductive material are buried" in the context of remaining limitations of the claim.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rakesh K. Dhingra whose telephone number is (571)-272-5959. The examiner can normally be reached on 8:30 -6:00 (Monday - Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on (571)-272-1435. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Rakesh Dhingra

Parviz Hassanzadeh
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Art Unit 1763